Abstracts

An Ultra-High Speed DCFL Dynamic Frequency Divider

T. Ichioka, K. Tanaka, T. Saito, S. Nishi and M. Akiyama. "An Ultra-High Speed DCFL Dynamic Frequency Divider." 1989 Microwave and Millimeter-Wave Monolithic Circuits Symposium Digest 89.1 (1989 [MCS]): 61-64.

A new circuit of a DCFL (Direct Coupled FET Logic) dynamic frequency divider has been developed using 0.25µm gate inverted HEMTs. The divider is operated with a single signal input in a very wide frequency range from 1.8 GHz to 15 GHz with low power dissipation of 62mW. The maximum operating frequency of 26.5 GHz is obtained.

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